中国中车 CRRC

TMTC,TMTD 330

Ver：2020D

Thyristor,Diode Modules

Key Parameters

V_{RRM}	1600~1800	V
$I_{T(AV)}$	330	A
I_{TSM}	8.5	kA
V_{TO}	0.9	V
r_T	0.47	mΩ

Applications

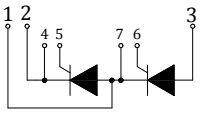
- Various rectifiers
- DC supply for PWM inverter
- Industry converter

- 3000 V_{RMS} isolating voltage with baseplate
- High power capability
- Industrial standard package

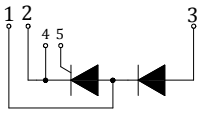
Voltage Ratings

Module Type	V_{DRM}/V_{RRM}(V)	Test Conditions
TMTC 330	1600 1800	T_{vj} = 25，130 °C $I_{DRM} = I_{RRM}$ = 70 mA $V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$ t_p = 10 ms $V_{DSM} = V_{DRM}$ $V_{RSM} = V_{RRM}$ + 100

TC



TD



Thermal & Mechanical Data

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
R_{thJC}	Thermal Resistance junction to case	sine.180°, per chip sine.180°, per module	-	-	0.11 0.055	°C / W
R_{thCH}	Thermal resistanc case to heatsink	per chip per module	-	-	0.04 0.02	°C / W
T_{vj}	Maximum junction operating temperature range		-40	-	130	°C
T_{stg}	Storage temperature		-40	-	120	°C
F	Busbar to module M8	Mounting torque ± 10 %	-	9	-	N·m
	Module to heatsink M6		-	6	-	N·m
W	Weight		-	0.8	-	kg

Current Ratings

$I_{T(AV)}$	Mean on-state current	Half Sine Wave, T_C=85°C	-	-	321	A
$I_{T(RMS)}$	RMS on-state current	T_C=85°C	-	-	504	A
I_{TSM}	Surge on-state current	t_p=10ms, Half Sine Wave, T_{vj}=130°C, V_R = 0	-	-	8.5	kA
I^2t	Limiting load integral	Sine Wave, t_p=10ms	-	-	36.1	10^4A^2s

Characteristics

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
V_{TM}	Peak on-state voltage	T_{vj} = 25 °C， I_{TM} = 750 A	-	-	1.45	V
I_{DRM} I_{RRM}	Forward leakage current Reverse leakage current	T_{vj} = 25 °C，130 °C， V_{DRM}/V_{RRM}	-	-	70	mA
V_{isol}	Isolation voltage	a.c.; 50 Hz; r.m.s. ; t=1min	-	3000	-	V
V_{TO}	Threshold voltage	T_{vj} = 130 °C	-	-	0.90	V
r_T	Slope resistance	T_{vj} = 130 °C	-	-	0.47	mΩ
I_H	Holding current	T_{vj} = 25 °C	-		200	mA
I_L	Latching current	T_{vj} = 25 °C	-	-	1000	mA

Dynamic Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
dv/dt	Critical rate of rise of off-state voltage	T_{vj} = 130 ℃， *Exp*. to 0.67 V_{DRM}	1000	-	-	V/μs
di/dt	Critical rate of rise of on-state current	T_{vj} = 130 °C， V_{DM} = 0.67 V_{DRM}， f = 50 Hz I_{TM} = 1000 A， I_{FG} = 2 A， t_r = 0.5 μs	-	-	250	A/μs
t_q	Turn-off time	T_{vj} = 130 °C， V_{DM} = 0.67 V_{DRM}， I_T = 1000 A *dv/dt* = 20 V /μs， V_R = 200 V， *-di/dt* = 10 A/μs	-	150	-	μs
Q_{rr}	Reverse Recovery Charge	T_{vj} = 130 °C， *-di/dt* = 10 A/μs， I_T = 1000 A， V_R = 200 V	-	1500	-	μC

Gate Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
I_{GT}	Gate trigger current	T_{vj} = 25 ℃	-	-	300	mA
V_{GT}	Gate trigger voltage	T_{vj} = 25 ℃	-	-	3	V
V_{GD}	Gate non-trigger voltage	T_{vj} = 130 ℃， V_D = 0.4V_{DRM}	0.3	-	-	V
V_{FGM}	Peak forward gate voltage		-	-	12	V
V_{RGM}	Peak reverse gate voltage		-	-	5	V
P_{GM}	Gate peak power losses		-	-	20	W
$P_{G(AV)}$	Gate average power losses		-	-	4	W

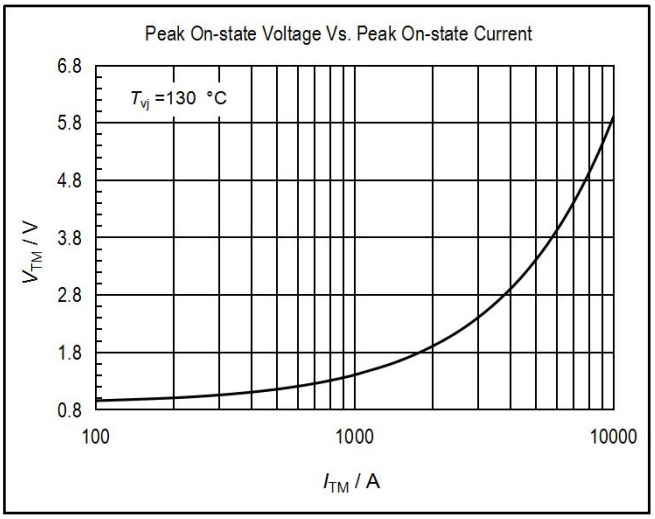


Fig1. Peak on-state Voltage Vs. Peak On-state Current

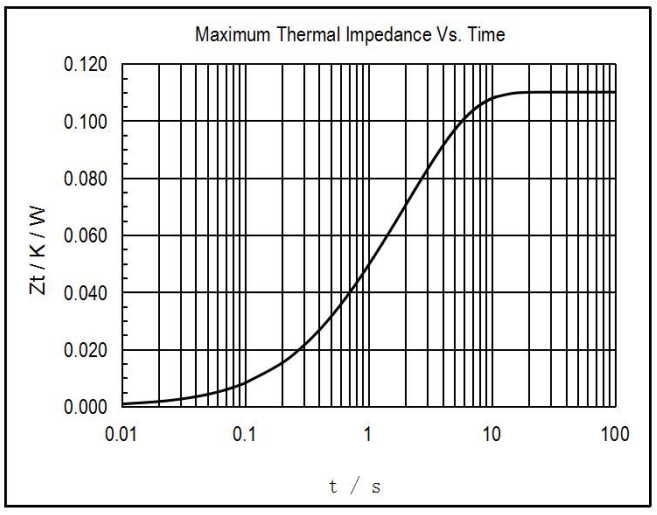


Fig2. Transinent thermal Impedance Vs. Time

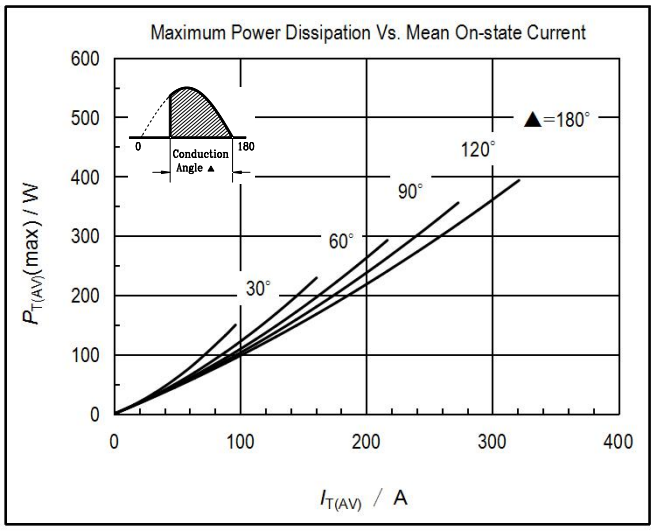


Fig3. Maximum Power Dissipation Vs. Mean On-state Current

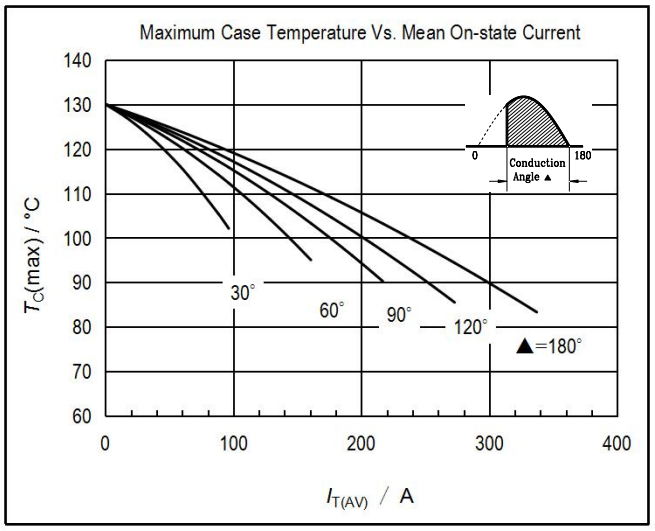


Fig4. Maximum Case Temperature Vs. Mean On-state Current

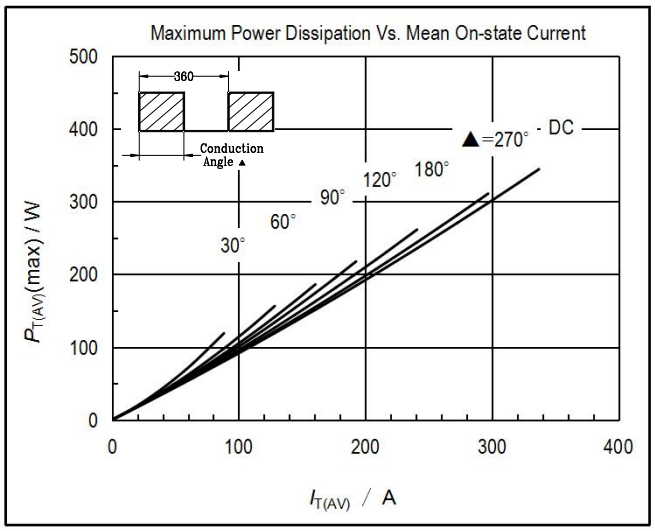


Fig5. Maximum Power Dissipation Vs. Mean On-state Current

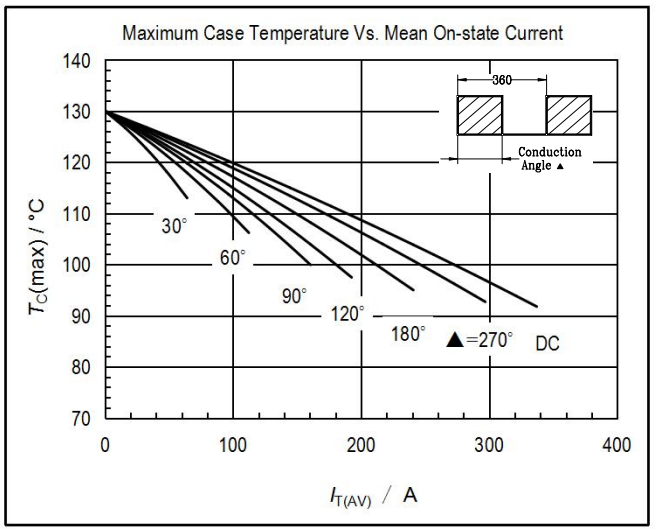


Fig6. Maximum Case Temperature Vs. Mean On-state Current

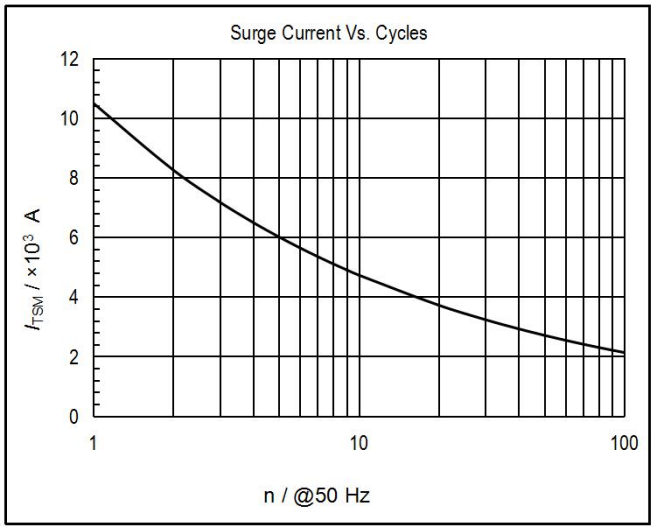


Fig7. Surge Current Vs. Cycles

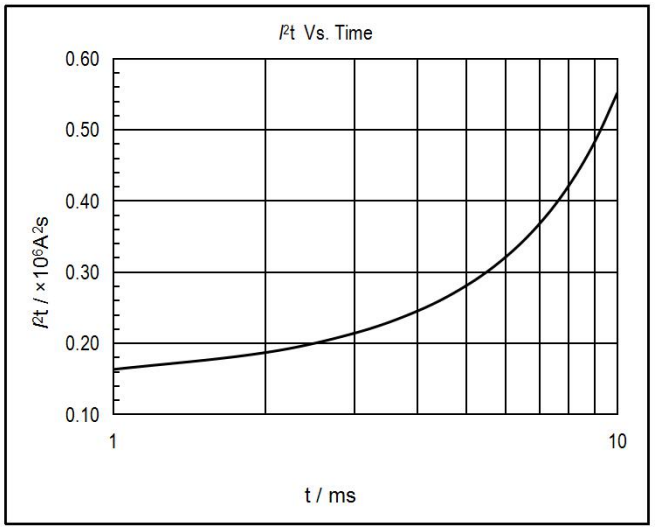


Fig8. I^2t Vs. Time

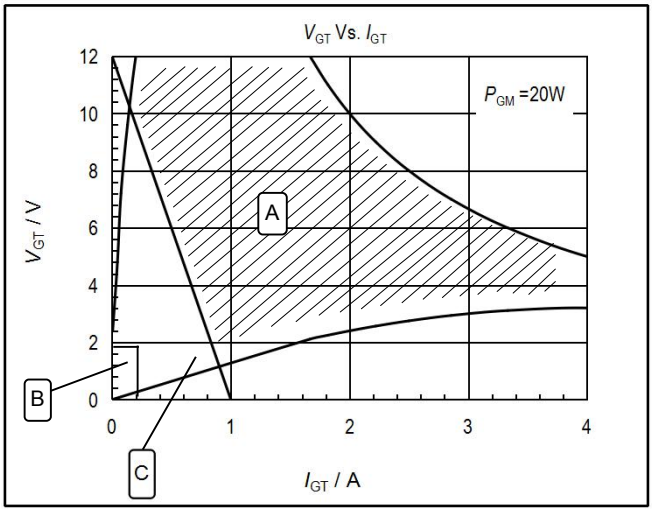


Fig9. V_{GT} Vs. I_{GT}

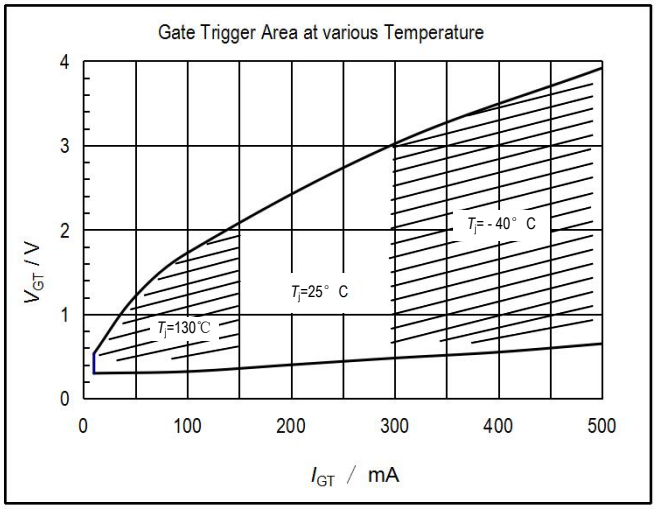


Fig10. Gate Trigger Area at various Temperature

A is Recommended Triggering Area.
B is Unreliable Triggering Area.
C is Recommended Gate Load Line.

A 为可靠触发区.
B 为不可靠触发区.
C 为建议采用的门极负载线.

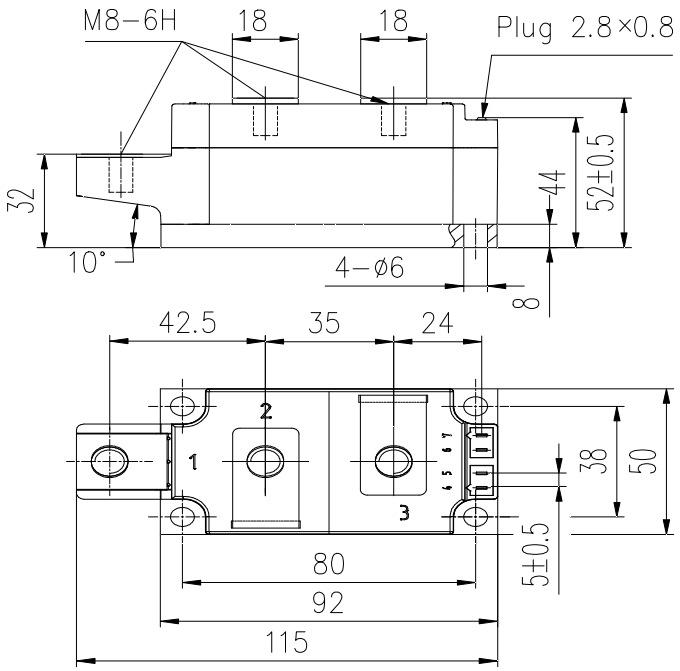


Fig9.Outline

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